

Concurrency Theory

Winter 2025/26

Lecture 8: The Alternating-Bit Protocol & Hennessy-Milner Logic

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<https://proglang.github.io/teaching/25ws/ct.html>

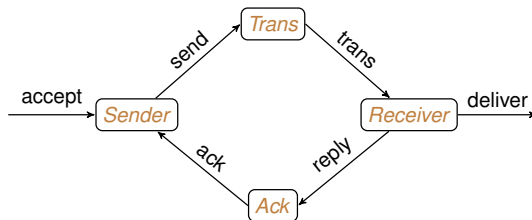
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Outline of Lecture 8

- 1 **Modelling the ABP**
- 2 Analysing the ABP
- 3 Modifying Channel Properties
- 4 Hennessy-Milner Logic (HML)

The Alternating-Bit Protocol (ABP)



Working principle of ABP

- Goal: **reliable communication** of data (from some finite set D) between *Sender* and *Receiver*.
- No direct communication between *Sender* and *Receiver*; all messages must travel through the **channels** (which are unreliable).
- *Sender* transfers data to *Receiver* via **transport channel** *Trans*.
- *Receiver* confirms reception via **acknowledgement channel** *Ack*.
- In addition to the actual data transmitted, a **control bit** is used to ensure reliability. After each successful transmission, this bit toggles its value ("Alternating-Bit Protocol").

The Channels

- Channels are **unidirectional** and can transfer only one message each time (i.e., **no message overtaking** is possible).
- Channels are **unreliable**, i.e., messages can be lost, corrupted, or duplicated. However transmission errors are **detected**.

The channel processes

- *Trans* transmits **frames** of the following form (where $\mathbb{B} := \{0, 1\}$):

$$F = \{db \mid d \in D, b \in \mathbb{B}\}.$$

- It detects transmission errors and reports them to *Receiver*:

$$Trans = \sum_{f \in F} send_f. (\overline{trans_f}.Trans + \overline{trans_{\perp}}.Trans)$$

- *Ack* behaves like *Trans* but only carries control bits:

$$Ack = \sum_{b \in \mathbb{B}} reply_b. (\overline{ack_b}.Ack + \overline{ack_{\perp}}.Ack)$$

The Sender

- After accepting data, *Sender* sends it via *Trans* with a control bit *b* (which is initially set to 0) repeatedly until the acknowledgement *b* is received over *Ack*. For the next data item, control bit $1 - b$ is used, and so on.
- When *Sender* receives an acknowledgement containing the same bit as the message it is currently transmitting, it stops transmitting that message, flips the protocol bit, and repeats the protocol for the next message.
- Otherwise, it re-initiates transmission.

The sender process

For $d \in D$ and $b \in \mathbb{B}$:

$$Sender = Send_0$$

$$Send_b = \sum_{d \in D} accept_d . Send_{db}$$

$$Send_{db} = \overline{send_{db}} . Wait_{db}$$

$$Wait_{db} = ack_b . Send_{1-b} + ack_{1-b} . Send_{db} + ack_{\perp} . Send_{db}$$

The Receiver

- *Receiver* gets the data item with a control bit b or the information that the data is corrupted.
- In the first case, if b is the expected value of the control bit (which is initially set to 0 also on the receiving side), b is returned via *Ack*.
- Otherwise, the transmission is re-initiated by returning the “wrong” control bit $1 - b$ to Sender.
- When a message is received for the first time, *Receiver* delivers it, while subsequent messages with the same control bit are simply acknowledged.

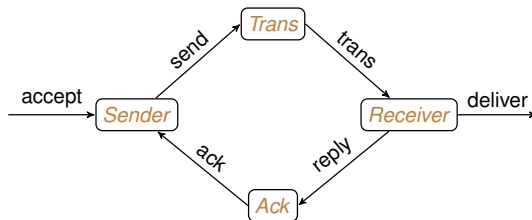
The receiver process

For $d \in D$ and $b \in \mathbb{B}$:

$$\text{Receiver} = \text{Recv}_0$$

$$\begin{aligned} \text{Recv}_b &= \sum_{d \in D} \text{trans}_{db} . \overline{\text{deliver}_d} . \overline{\text{reply}_b} . \text{Recv}_{1-b} \\ &\quad + \sum_{d \in D} \text{trans}_{d(1-b)} . \overline{\text{reply}_{1-b}} . \text{Recv}_b \\ &\quad + \text{trans}_{\perp} . \overline{\text{reply}_{1-b}} . \text{Recv}_b \end{aligned}$$

The Overall Protocol



- The only actions visible to the environment are *accept* and *deliver* steps on the *Sender* and *Receiver* side, respectively; everything else is considered to be internal communication.
- The protocol is expected to **behave like a one-place buffer**.

The protocol and its specification

$$ABP = (Sender \parallel Trans \parallel Ack \parallel Receiver) \setminus L$$

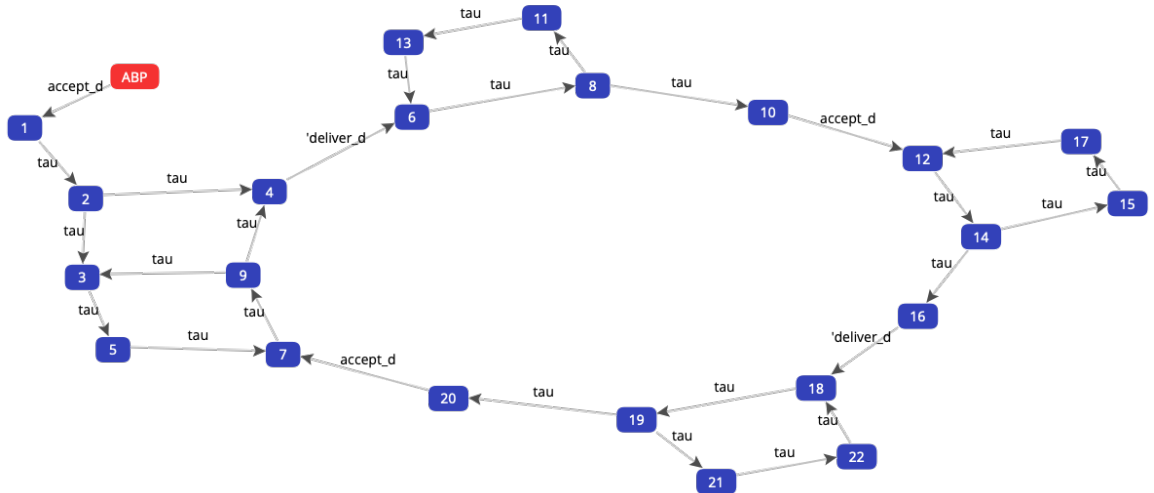
$$L = \{send_{db}, trans_{db} \mid d \in D, b \in \mathbb{B}\} \\ \cup \{reply_b, ack_b \mid b \in \mathbb{B}\} \cup \{trans_{\perp}, ack_{\perp}\}$$

$$Spec = \overline{accept_d.deliver_d}.Spec$$

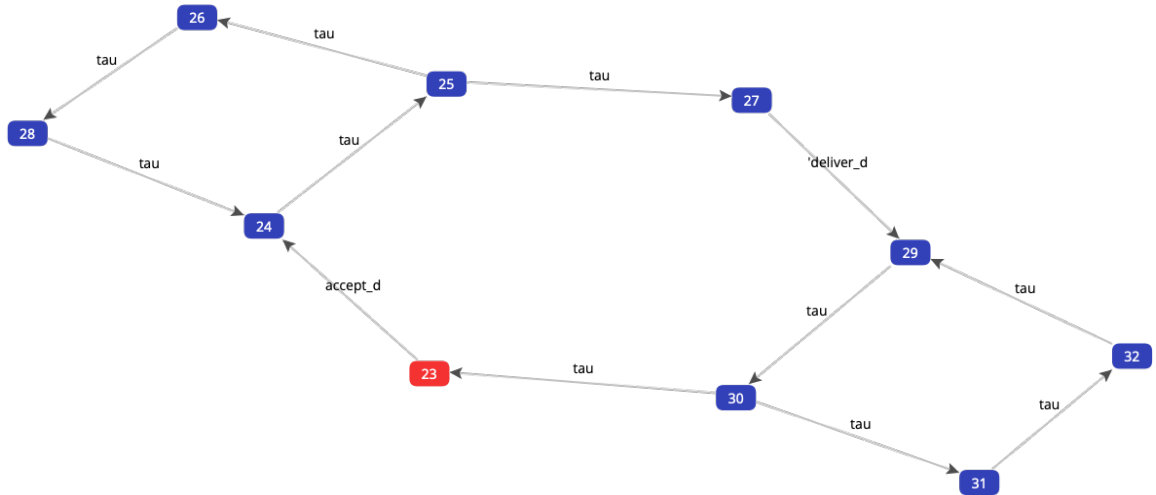
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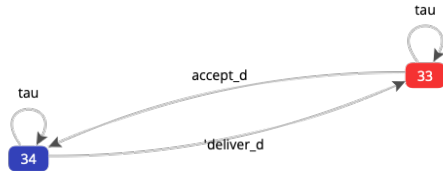
The State Space



The State Space Modulo Strong Bisimulation



The State Space Modulo Weak Bisimulation



Properties

Correctness

The protocol and its specification are **weakly bisimilar**:

$$ABP \approx Spec.$$

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Absence of deadlocks

ABP is **deadlock free** (formal details later):

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Existence of livelocks

ABP **contains livelocks** (formal details later):

$$\begin{aligned} ABP &\models HasLivelock \\ HasLivelock &\stackrel{min}{=} CanDiverge \vee \langle Act \rangle HasLivelock \\ CanDiverge &\stackrel{max}{=} \langle \tau \rangle CanDiverge \end{aligned}$$

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Modifying Channel Properties

Lossy channels (without detection)

$$\begin{aligned} Trans &= \sum_{f \in F} send_f. (\overline{trans_f}. Trans + \tau. Trans) \\ Ack &= \sum_{b \in \mathbb{B}} reply_b. (\overline{ack_b}. Ack + \tau. Ack) \end{aligned}$$

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Effects:

- $ABP \not\approx Spec$ (ABP only weakly simulates $Spec$)
- $ABP \not\models NoDeadlock$ (both $Sender$ and $Receiver$ waiting but channels empty)
- $ABP \not\models HasLivelock$ (never re-initiates transmission)

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Duplicating channels (without detection)

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Effects:

- $ABP \not\approx Spec$ (ABP only weakly simulates $Spec$)
- $ABP \not\models NoDeadlock$
- $ABP \not\models HasLivelock$ (only bounded re-transmission)

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Verifying Correctness of Concurrent Systems

Equivalence-checking approach

$$Impl \equiv Spec$$

- \equiv is some equivalence, e.g., \sim or \approx^c .
- *Spec* is often expressed in the same language as *Impl*, e.g., CCS.
- *Spec* provides the **full** specification of the intended behaviour.

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Model-checking approach

$$Impl \models Prop$$

- \models is the satisfaction relation.
- *Prop* is a particular feature, often expressed via a logic, e.g., HML.
- *Prop* is a **partial** specification of the intended behaviour.

Goal: check processes for **simple properties**

- Action *a* is initially enabled.
- Action *b* is initially disabled.
- A deadlock never occurs.
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Goal: check processes for **simple properties**

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Approach:

- Formalisation in **Hennessy-Milner Logic (HML)**
- M. Hennessy, R. Milner: *On Observing Nondeterminism and Concurrency*, ICALP 1980, Springer LNCS 85, 299–309
- Checking by **exploration of state space**

Definition 8.1 (Syntax of HML)

(Hennessy & Milner 1985)

The set HMF of **Hennessy-Milner formulae** over a set of actions Act is defined as follows:

$F ::= tt$	(true)
ff	(false)
$F_1 \wedge F_2$	(conjunction)
$F_1 \vee F_2$	(disjunction)
$\langle \alpha \rangle F$	(diamond)
$[\alpha] F$	(box)

where $\alpha \in Act$.

Meaning of HML Constructs

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Abbreviations for $L = \{\alpha_1, \dots, \alpha_n\}$ ($n \in \mathbb{N}$):

- $\langle L \rangle F := \langle \alpha_1 \rangle F \vee \dots \vee \langle \alpha_n \rangle F$
- $[L] F := [\alpha_1] F \wedge \dots \wedge [\alpha_n] F$
- In particular, $\langle \emptyset \rangle F := \text{ff}$ and $[\emptyset] F := \text{tt}$.
- Thus, a process satisfies
 - $\langle \text{Act} \rangle \text{tt}$ iff it has some outgoing transition, i.e., is not deadlocked, and
 - $[\text{Act}] \text{ff}$ iff it has no outgoing transition, i.e., is deadlocked.

Definition 8.2 (Semantics of HML)

Let $(S, Act, \longrightarrow)$ be an LTS and $F \in HMF$.

The set of processes in S that **satisfy** F , $\llbracket F \rrbracket \subseteq S$, is defined by:

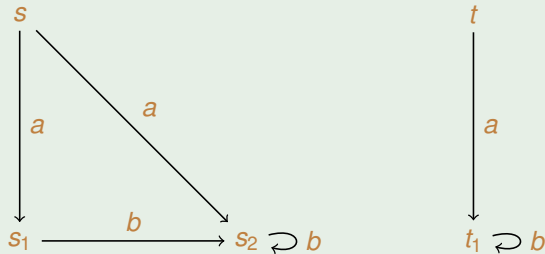
$$\begin{aligned}\llbracket tt \rrbracket &:= S & \llbracket ff \rrbracket &:= \emptyset \\ \llbracket F_1 \wedge F_2 \rrbracket &:= \llbracket F_1 \rrbracket \cap \llbracket F_2 \rrbracket & \llbracket F_1 \vee F_2 \rrbracket &:= \llbracket F_1 \rrbracket \cup \llbracket F_2 \rrbracket \\ \llbracket \langle \alpha \rangle F \rrbracket &:= \langle \cdot \alpha \cdot \rangle (\llbracket F \rrbracket) & \llbracket [\alpha] F \rrbracket &:= [\cdot \alpha \cdot] (\llbracket F \rrbracket)\end{aligned}$$

where $\langle \cdot \alpha \cdot \rangle, [\cdot \alpha \cdot] : 2^S \rightarrow 2^S$ are given by

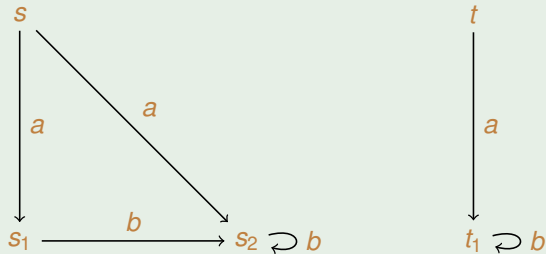
$$\begin{aligned}\langle \cdot \alpha \cdot \rangle (T) &:= \{s \in S \mid \exists s' \in T : s \xrightarrow{\alpha} s'\} \\ [\cdot \alpha \cdot] (T) &:= \{s \in S \mid \forall s' \in S : s \xrightarrow{\alpha} s' \Rightarrow s' \in T\}\end{aligned}$$

We write $s \models F$ iff $s \in \llbracket F \rrbracket$. Two HML formulae are **equivalent** (written $F \equiv G$) iff they are satisfied by the same processes in every LTS.

Example 8.3 ($\langle \cdot \alpha \cdot \rangle$, $[\cdot \alpha \cdot]$ operators)

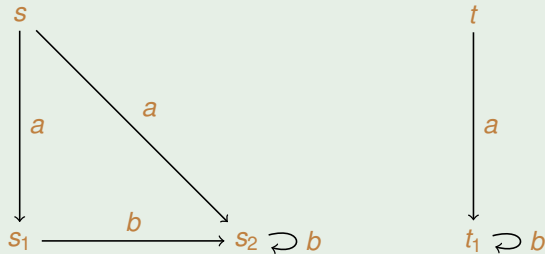


Example 8.3 ($\langle \cdot \alpha \cdot \rangle$, $[\cdot \alpha \cdot]$ operators)



$$(1) \ \langle \cdot a \cdot \rangle(\{s_1, t_1\}) = \{s, t\}$$

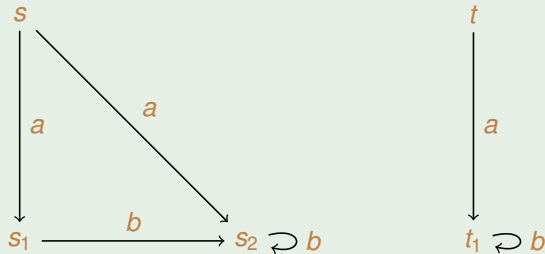
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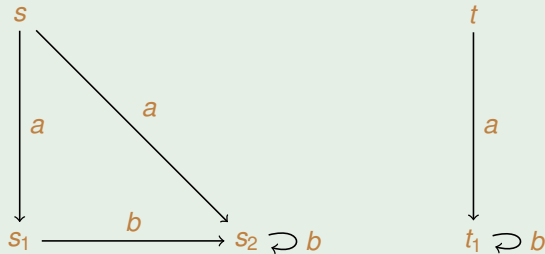
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- (4) $[\cdot b \cdot](\{s_1, t_1\}) = \{s, t, t_1\}$

Example 8.4

(1) Action a is initially enabled: $\langle a \rangle \text{tt}$

$$\begin{aligned} \llbracket \langle a \rangle \text{tt} \rrbracket &= \langle \cdot a \cdot \rrbracket \llbracket \text{tt} \rrbracket \\ &= \langle \cdot a \cdot \rrbracket (S) \\ &= \{s \in S \mid \exists s' \in S : s \xrightarrow{a} s'\} =: \{s \in S \mid s \xrightarrow{a}\} \end{aligned}$$

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(2) Action b is initially disabled: $[b] \text{ff}$

$$\begin{aligned} \llbracket [b] \text{ff} \rrbracket &= [\cdot b \cdot] \llbracket \text{ff} \rrbracket \\ &= [\cdot b \cdot] (\emptyset) \\ &= \{s \in S \mid \forall s' \in S : s \xrightarrow{b} s' \Rightarrow s' \in \emptyset\} \\ &= \{s \in S \mid \nexists s' \in S : s \xrightarrow{b} s'\} =: \{s \in S \mid s \not\xrightarrow{b}\} \end{aligned}$$

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(1) Absence of deadlock:

- initially: $\langle \text{Act} \rangle \text{tt}$
- always: later
(requires recursion)

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(1) Absence of deadlock:

- initially: $\langle \text{Act} \rangle \text{tt}$
- always: later
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(2) Responsiveness:

- initially:
 $[request] \langle \overline{reply} \rangle \text{tt}$
- always: later
(requires recursion)